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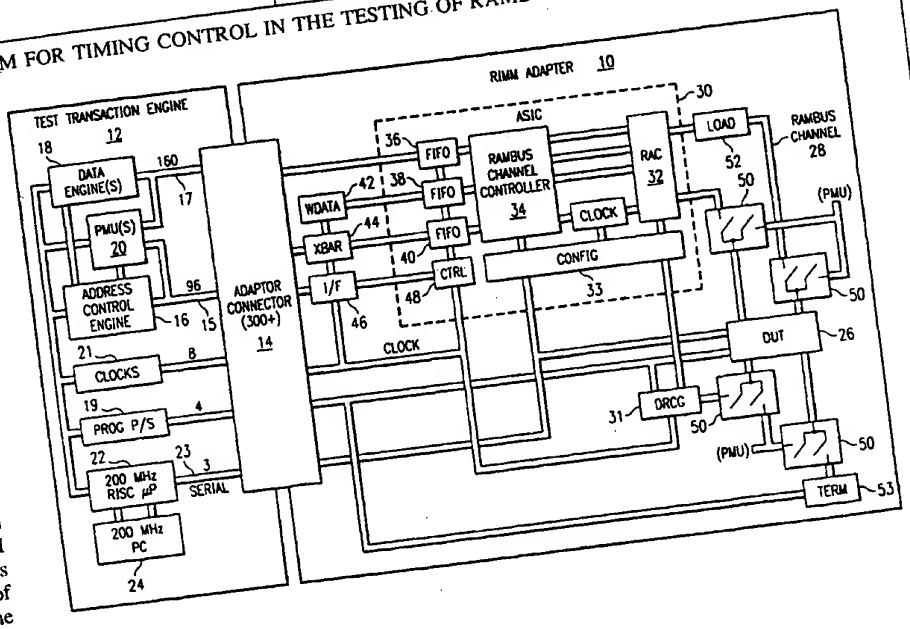
(57) Abstract

A system and method for testing a RIMM loaded with RDRAM integrated circuits generates and reads test transaction data with a test transaction engine, such as a microprocessor-based memory tester. A RIMM adapter interfaces with the test transaction engine and the RIMM under test to communicate test data, including test write, address, control and read data. A comparison of test read data returned to the test transaction engine from the RIMM against predetermined values allows a determination of the operational status of the RIMM. A load circuit skews the clock timing signal by a programmable amount relative to a constant data signal to allow testing of setup and hold time, and simulation of various trace length conditions. The RIMM adapter is embodied as an ASIC with plural FIFO circuits interfaced between the test transaction engine and a channel controller and RAC. The FIFOs reconcile differences in timing between generation and return of test data and demands by the RAC and channel controller. Separate read and write data paths between the test transaction engine and ASIC support improved rates of data transfer. The test transaction engine provides full speed test transactions by using instruction data to generate test data with FPGAs.



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METHOD AND SYSTEM FOR TIMING CONTROL IN THE TESTING OF RAMBUS MEMORY MODULES

TECHNICAL FIELD OF THE INVENTION

This invention relates in general to the field of testing electronic devices, and more particularly to timing control in the testing of memory modules.

BACKGROUND OF THE INVENTION

Memory integrated circuits are typically assembled on memory modules for incorporation into computing devices, such as personal computers. Before a memory module is incorporated in a computing device, the module and memory integrated circuits assembled on the module are usually tested for faults. For instance, personal computer manufacturers typically purchase memory modules from subcontractors. The subcontractors assemble the memory integrated circuits on the memory modules according to the manufacturers' specifications, and then test the modules to ensure their proper operation before shipping the modules to the manufacturer. Computer manufacturers expect high reliability for the memory modules. Thus, subcontractors who assemble memory modules generally must test the assembled modules to meet predetermined specifications of the computer manufacturer with a high degree of reliability.

Conventional memory integrated circuits include DRAM, SDRAM, and SGRAM integrated circuits that operate at speeds of up to 100 megahertz. Recently, a new type of integrated memory circuit known as a direct RAMBUS integrated circuit (RDRAM), has been introduced that is capable of operating at much higher speeds, such as a clock speed of 400 megahertz, with data transactions occurring on both edges of the clock signal to provide an effective device speed of 800 megahertz. To obtain these improved operating speeds, RAMBUS integrated circuits are loaded on a specially designed RDRAM integrated memory module, known as a RAMBUS In-Line Memory Module ("RIMM"). RIMMs include a Direct RAMBUS ASIC channel cell (RAC) to support communications between the RIMM and another RAC located in a computing device. A RAC is a logical to physical interface that multiplexes and demultiplexes 144 bit wide datums with an 18 bit wide RAMBUS channel. Cooperating RACs communicate data over the 18 bit wide RAMBUS channel by exchanging control and address information in unique packetized formats. A RAMBUS Memory Controller ("RMC") supports data transfers with a RAC by taking simple high-level commands and data to create simpler commands formatted for the RAC and by scheduling for data transmittal or retrieval.

For instance, a RMC may receive or transmit data at a 100 MHz clock rate. In one clock cycle, the RMC may receive 40 bits worth of information, including 35 address bits, 4 command bits and 1 packet length bit, along with 144 bits worth of data to be written to a RIMM. The RMC reformats the 40 address/command/length bits into a sequence of commands to the RAC with each command having 64 bits of packet information and 12 bits of scheduling information. The 144 bits of data are passed unchanged to the RAC. The RAC then transmits this information to a RAC of one of the Direct RDRAM chips in the RIMM with the 64 bits of packet information broken

down into 8 sets of 8 bits and the 144 bits of data broken down into 8 sets of 18 bits. The transfer between RACs is clocked out on the leading and trailing edges of a 400 MHz clock to allow all eight sets of data to be transmitted within a 10ns window that matches the 100 MHz system bus clock.

The use of RDRAM integrated circuits loaded on a RIMM allows a substantial increase in the rate at which data is exchanged for use by a processor of a computing device. However, the increased speed at which RIMMs operate makes it especially important to ensure that no faults exist on the RIMMs before the RIMMs are used in a computing device. At the present time, commercial microprocessor bus systems do not exist that will support a RAMBUS channel operating at higher than 100 megahertz.

Faults associated with a RIMM can be introduced in a number of different manners. A fault can exist in the RDRAM integrated circuits and RIMM printed wire board (PWB) before assembly, or can be introduced during assembly. For instance, RIMM PWBs can have PWB faults such as open or shorted traces due to under plating or over plating, excessive warpage, and out of tolerance electrical characteristics. RDRAM faults can include open or shorted pins due to lead frame bonding flaws, inoperable nodes internal to the device, and excessive sensitivity to signal patterns, temperature variations, voltages, and/or internal node states. Faults introduced during assembly of a RIMM can include incorrect installation of parts, open or shorted signals through the use of excessive or insufficient solder, signal path contamination resulting in high pin leakage, ESD damage resulting in high pin leakage, and damaged pin drivers or input buffers.

Several conventional testers are available for testing memory modules. The simplest type of memory tester is a microprocessor-based tester. Microprocessor-

based testers essentially act as a mother board to pass microprocessor-generated test data to a module and read the test data sent back from the module. The memory module is tested by comparing the written and read data. Although microprocessor-based testers are simple to build and use, they are generally slow in operation and incapable of performing more complex types of tests. Such testers usually feature commodity memory controllers as the interface between the microprocessor and the memory module.

Most other types of conventional memory testers are hardware-enhanced. Hardware-enhanced testers provide more rapid testing of memory modules by using specialized hardware to generate test accesses and verify test data. One such hardware-enhanced memory testing system is a vector-based system. Vector-based systems use a microprocessor to generate test data, and then store the test data in memory until the data is sent to the module under test. A key disadvantage to vector-based systems is that they generally require large amounts of memory for storing test data before the data is sent to the module under test.

Another hardware-enhanced method for testing memory modules is through the use of an interface that provides test data to the module under test. For instance, the SIGMA testing systems produced by Tanisys Technology, Inc. create test data with algorithms and incorporate specialized controllers to interface the algorithmically-created data with the module under test. A microprocessor supervises the operation of the specialized controller, which in response generates and writes predetermined data to the memory module through an interface, and then reads back the data and compares it against the written data to ensure that the memory module is operating properly.

Many of the hardware-enhanced memory testers use pin drivers. Pin drivers and receivers interfaced with

the memory module send signals to and receive signals from the memory module under test. Conventional pin drivers are frequently used to test a variety of integrated circuits, including microprocessors, where operational parameters such as input voltage range, output voltage range, power supply range, and signal timing vary widely between device types. Pin-driver based testers generally incorporate expensive and complex hardware and software that determine whether the output signals generated are appropriate for a given suite of test signals. Conventional pin drivers are expensive and their use to test memory devices is generally considered overkill since memory devices typically operate over a narrow range of voltages and speeds, such as the 0.8 voltage swing for RDRAM signals, whereas pin drivers are designed to operate over a large voltage range, such as 7 to -5 volts. In addition, conventional pin drivers are typically housed in large packages with high input voltages that generate considerable amounts of heat, frequently requiring cooling by fluids.

A number of difficulties exist in attempting to use conventional memory testing systems to test RIMMs. One difficulty is presented by the rapid operating speeds of RIMMs. For instance, conventional 100 megahertz memory devices and busses cannot exchange data at the full operating rate of a RIMM. Although pin-driver systems can present data to a RIMM at full operating speeds, pin driver systems are expensive and difficult to use.

Another difficulty is converting data generated by conventional testing systems into a format that is readable by a RIMM. For instance, RIMMs typically have 8 control lines that carry packetized control information in 64 bit packets. Further, RIMMS have an 18 bit wide RAMBUS channel with occupancy of the channel dependent upon prior and pending channel activity.

Another difficulty is the implementation of testing algorithms and sequences that test the various RIMM configurations and RIMM transaction sequences under worst-case test conditions.

SUMMARY OF THE INVENTION

Therefore a need has arisen for a memory testing system and method which will support inexpensive testing of RIMMs with at-speed test data.

A further need has arisen for a memory testing system and method which maintains full utilization of a RAMBUS channel to test the RIMM at full operating speeds.

A further need has arisen for a memory testing system and method which supports testing of a variety of RIMM configurations under a variety of test conditions.

A further need has arisen for programmable testing of clock skew for transfer of valid data at appropriate clock edges.

In accordance with the present invention, a memory testing system and method is provided that substantially eliminates or reduces disadvantages and problems association with previously developed memory testing systems and methods. A RIMM adapter accepts test data for transfer to and from a RIMM to allow evaluation of the RIMM's operation.

The RIMM adapter includes an application specific integrated circuit (ASIC) having a RAC that multiplexes and demultiplexes test data with a RAMBUS channel. The RAMBUS channel is controlled by a channel controller located on board the ASIC in communication with the RAC. The channel controller writes and reads data from one or more first-in-first-out (FIFO) circuits also located on board the ASIC. The FIFOs form the interface between the ASIC of the RIMM adapter and a test transaction engine.

In one embodiment, the test transaction engine is a hardware-enhanced based memory tester.

In another embodiment, a test transaction engine located on the RIMM adapter generates and compares test data based on instructions provided to processing circuits, such as field programmable gate arrays. A sequencer in communication with write data generate, address/command generate and read data compare engines supports transfer of test transaction data between the FIFOs and the test transaction engine. The FIFOs allow the RAC to provide the RIMM data transactions at full operating speed. Registers located on the ASIC of the RIMM adapter are in communication with the channel controller and RAC to allow modifications of the operational characteristics of the channel controller and RAC to support control of channel drive strengths and timing. A parametric measurement unit (PMU) and a load unit interface with the RIMM to provide analog testing signals and simulated loads.

In one embodiment the load unit provides programmable skewing of clock signals relative to data signals to test valid data slot specifications. The load unit skews the clock signal in programmable time increments to test either the setup or hold time of data transactions. The programmable clock delay supports testing of data transactions at integral multiples of clock edges and then supports calibration of timing margins within a given clock edge.

Instructions for test data transactions are provided by a host computer in communication with the test transaction engine. The instructions are stored in a SRAM, and identify the type of transactions to be performed with the RIMM. A sequencer communicates with the SRAM and with the host computer, a read compare engine, a write generate engine, and an address command generate engine. The sequencer supplies addresses to the

SRAM in a user defined order to have the write generate and address command generate engines generate both transaction address commands and test write data for transfer to the RIMM, or to have the read compare engine verify data returned from the RIMM. Instructions from the SRAM direct the sequencer to modify the address, test write data, and read compare data after a transaction is issued to support a high data flow rate to the RIMM.

The read compare engine and write generate engines have separate data paths for communicating with the RIMM adapter ASIC. The channel controller of the ASIC accepts data from the write generate engine through a write FIFO for transmission to the RIMM as the RAMBUS channel is available, and provides data received from the RAMBUS channel to a read FIFO for transmission to the read compare engine. The read compare engine compares data received from the RIMM with expected data values and issues status results back to the sequencer and host computer.

In one embodiment, the read compare engine, write generate engine and address command generate engine are field programmable gate arrays (FPGAs), having a bank of registers sharing a single arithmetic logic unit to provide interleaved accesses that help ensure uninterrupted data flow to and from the RIMM.

In another embodiment, the RIMM adapter ASIC includes a bypass circuit that allows direct communication between the test transaction engine and the RAC loaded on the ASIC. The bypass mode allows direct communication of test transaction data from the tester to the RAC without processing by the channel controller loaded on the ASIC. Thus, for instance, the test transaction engine may provide 64 bit commands and 144 bit data directly to the RAC on the ASIC to test failure modes in the field with a logic analyzer.

The present invention provides a number of important technical advantages. One important technical advantage is that the RIMM adapter implements transaction sequences for testing a RIMM at full speed when supplied with transaction commands issued by lower-speed testing engines. For instance, 100 megahertz, 144 bit datum transactions are provided to the 18 bit RIMM channel through the RIMM adapter to facilitate full control of transaction sequences. Further, the transactions are not constrained by microprocessor or memory controller implementations.

Another important technical advantage of the present invention is that full utilization of the RIMM channel is maintained. The RIMM channel is tested at full speed, such as its 800 megahertz operating speed, by transactions provided through the RIMM adapter. Separate read and write paths provide double the speed of a single read and write path and avoids waiting for host bus turnaround. Further, by locating a memory controller on board an ASIC instead of in the test engine, and providing test data through FIFO circuits before assigning the test data to memory channels, the time for transferring data to the RIMM is reduced.

Another advantage of the present invention is that it supports a variety of RIMM configurations tested under a variety of conditions. The channel controller supports control of channel drive strengths and timing to adjust data and clock skew. For instance, the channel controller allows testing with different numbers of RDRAM parts loaded on a RIMM, and with delays in clocking rate that may be associated with changes in bus length. The load unit simulates operational conditions to ensure the RIMM meets worst case test conditions, including simulation of multiple RIMMS loaded on a RAMBUS channel. The programmable load unit enables precise programmable testing of system specifications associated with timing

errors introduced by factors such as clock jitter and trace length errors, such as propagation delays, loading, characteristic impedance and reflection.

Another important technical advantage of the present invention is that the test transaction engine may communicate directly with the RAC through the bypass circuit. By configuring the ASIC so that the channel controller is bypassed, all possible memory access methods for talking to the RIMM may be utilized, which allows for the testing of additional sequences of RAC commands that may cause failures.

BRIEF DESCRIPTION OF THE DRAWINGS

A more complete understanding of the present invention and advantages thereof may be acquired by referring to the following description taken in conjunction with the accompanying drawings in which like referenced numbers indicate like features and wherein:

FIGURE 1 depicts a block diagram of a RIMM adapter interfaced with a test transaction engine;

FIGURE 2 depicts a block diagram of a RIMM adapter and test transaction engine in a stand-alone, contiguous-unit configuration;

FIGURE 3 depicts a block diagram of an address command generate engine;

FIGURE 4 depicts a block diagram of a read compare engine;

FIGURE 5 depicts a block diagram of an address crossbar switch;

FIGURE 6 depicts a channel controller bypass circuit;

FIGURE 7 depicts a block diagram of a RIMM tester in a channel controller bypass configuration;

FIGURE 8 depicts a flow diagram of a memory testing sequence; and

FIGUREs 9A and 9B depict a programmable load unit and associated timing information.

DETAILED DESCRIPTION OF THE INVENTION

Preferred embodiments of the present invention are illustrated in the FIGURES, like numeral being used to refer to like and corresponding parts of the various drawings.

Hardware-enhanced memory testing systems provide inexpensive but accurate testing of memory modules. For instance, the SIGMA memory testing system sold by Tanisys Technology, Inc. accepts user-specific testing sequences that support the running of a predetermined series of read and write cycles on a memory module to ensure that the memory module operates correctly. Hardware-enhanced memory testing systems support full speed operational testing of conventional memory, such as 100 MHZ SDRAM, DRAM and SGRAM, by using commodity high speed interfaces which operate at 100 MHZ. However, conventional hardware-enhanced memory testing systems are not able to directly interface with RIMMs having RDRAM integrated circuits at full operational speeds due to the unique data format used by RIMMs and due to the rapid operating speeds at which data is transferred by RIMMs.

Referring now to Figure 1, a block diagram of a RIMM adapter 10 is interfaced with a test transaction engine 12 by an adapter connector 14. RIMM adapter 10 and test transaction engine 12 could alternatively be interfaced across a distance by conventional connectors and cables. RIMM adapter 10 provides an interface to accept test transaction data from test transaction engine 12 for testing a RIMM loaded in a device under test (DUT) adapter 26. Adapter connector 14 is a 300 pin connection

that supports two separate data paths between RIMM adapter 10 and test transaction engine 12. Thus, a write data path 15 provides up to 96 bits of test write data, address and control data instructions from test transaction engine 12 to RIMM adapter 10, and a separate read data path 17 accepts up to 160 bits of test read data from RIMM adapter 10 to test transaction engine 12. The use of separate write and read data paths effectively doubles the amount of data that can be transferred between RIMM adapter 10 and test transaction engine 12.

Test transaction engine 12 is a hardware-enhanced memory test system, such as the SIGMA 3 memory test system sold by Tanisys Technology, Inc. The Sigma 3 memory test system is operable to test standard memory modules loaded with up to 160 data bit SRAM, DRAM or SGRAM that generally operate at speeds of up to 100 megahertz.

Test transaction engine 12 provides a user interface, such as a personal computer 24 with a 200 MHz processor. Personal computer 24 communicates with a 200 MHz RISC processor 22 loaded on test transaction engine 12, to accept test inputs and display test results. For a RIMM under test on DUT 26 of RIMM adapter 10, test transaction engine 12 provides RIMM adapter 10 with power through programmable power source 19. Test transaction engine 12 also provides RIMM adapter 10 with access test address and control data and test write data through address control engine 16, and with read compare functionality through data engine 18. Address control engine 16 generates the access test address and control signals that specify the location in the RIMM to which test data is written and from which test data is read. Address control engine 16 also provides instructions for the creation of test write data for transfer to the RIMM, and creation of read compare data for comparison with test data read from the RIMM. Data engine 18 generates

test data for comparison with read test data from the RIMM, enabling a comparison of the read test data against expected results. If data from the RIMM does not match expected results, data engine 18 identifies the error for display to the user.

Other test signals provided by test transaction engine 12 include signals provided to parametric measurement unit (PMU) 20. PMU 20 includes circuitry to perform current leakage, DC voltage and resistance measurements of the RIMM. A serial interface 23 with RISC processor 22 supports initialization of a RIMM for accepting test transactions. A clock 21 provides timing signals for coordination of data transfers. Processor 22 interfaces with a personal computer 24 to accept test instructions and direct the operation of the test by test transaction engine 12.

RIMM adapter 10 acts as a docking adapter to supply a RIMM loaded in DUT adapter 26 with test data in a RAMBUS format at 800 MHZ operating speed through a RAMBUS channel 28. Essentially, RIMM adapter 10 operationally converts 144-bit wide 100 MHZ test data generated by test transaction engine 12 to supply 18-bit wide 800 MHZ test data to RAMBUS channel 28, and converts 18-bit wide 800 MHZ test data received from a RIMM in DUT 26 into 144-bit wide 100 MHZ test data for evaluation by test transaction engine 12.

Test data is provided to and received from RAMBUS channel 28 by an application specific integrated circuit (ASIC) 30. ASIC 30 includes a RAC 32, which is defined by the RAMBUS Corporation standards, a RAMBUS channel controller 34 in communication with RAC 32, and plural FIFO circuits 36, 38 and 40, in communication with RAMBUS channel controller 34. RAC 32 accepts test write data from channel controller 34 and formats the test write data for transfer to a RIMM via RAMBUS channel 28. RAC 32 also accepts test read data from a RIMM via RAMBUS

channel 28 and formats the test read data for transfer to test transaction engine 12 through channel controller 34. Channel controller 34 controls the flow of data through RAC 32 as RAMBUS channel 28 is available. A direct RAMBUS clock generator 31 communicates with clock 21 of test transaction 12, control circuit 48 of ASIC 30 and a configuration circuit 33 of ASIC 30, enabling alignment of clock signals of test transaction engine 12 and ASIC 30. Configuration circuit 33 includes registers to store data for enabling alternative configurations of RAC 32 and channel controller 34, such as clock control modes.

A read FIFO 36 accepts test read data from a RIMM in DUT 26 through controller 34 and provides the test read data to data engine 18 for comparison with expected results. A write FIFO 38 accepts data from a write data engine 42 and provides the data through RAC 32 to RIMM DUT 36. Thus, read FIFO 36 and write FIFO 38 provide read and write 144 bit data paths with ASIC 30, effectively doubling the transaction speed at which ASIC 30 can process 144 bit test write and test read datum.

An address cross-bar circuit 44 interfaces with address control engine 16 and with an address FIFO 40 to form contiguous address space from five separate fields, enabling a variety of RIMM configurations to be tested and to optimize test address sequencing. Address cross-bar circuit 44 accepts 35 address lines from address control engine 16 and outputs the 35 address lines to address FIFO 40. A control interface circuit 46 communicates with a control circuit 48 of ASIC 30 to provide control information for supporting time-aligned address and data information during RIMM transactions. Control interface circuit 46 includes registers to support transfer of miscellaneous control logic, such as control of isolation relays 50, which enable analog measurements. Control circuit 48 provides ASIC 30 with internal control logic based upon data received from

control interface 46. For instance, control circuit 48 provides control of data paths in ASIC 30 for loading and updating data in FIFOs 38 and 40, and transfer of data from FIFOs 38 and 40 to RAC 32 through channel controller 34.

Analog measurements of a RIMM loaded in DUT 26 are performed by PMU 20. Isolation relays 50 support electrical isolation of DUT 26 from other circuits on RIMM adapter 10 when PMU 20 performs analog measurements. PMU 20 includes a programmable current source and sink, a programmable voltage source, and a differential voltage analog-to-digital converter to perform current leakage, DC voltage and resistance measurements on a RIMM loaded in DUT 26.

A load circuit 52 is provided on RAMBUS channel 28 to attenuate channel signals for altering the electrical characteristics of RAMBUS channel 28 by, for instance, degrading the channel signal. For instance, load circuit 52 can vary the capacitance of RAMBUS channel 28 to subject a RIMM in DUT 26 to various test conditions, can simulate the effect of a second device interfaced with RAMBUS channel 28, and can simulate increased trace length of the bus. A termination circuit 53 supplies the RAMBUS-specified electrical termination of signals of channel 28.

FIGURE 9A depicts one embodiment of a load circuit 52 that provides programmable skewing of the clock timing signal relative to the data signal. FIGURE 9B depicts an associated exemplary timing signal 200. Timing signal 200 has a cycle time t_{clk} of 400 MHz with data transfers occurring twice per cycle, once at each clock edge, resulting in a data transfer rate of 800 MHz.

Typically, data is held valid for a period of approximately 650 ps with the center of the valid data generally located proximate to the associated clock edge. Data is brought to a valid value by at least a minimum

setup time, t_{setup}, before the clock edge, and held at a valid value for a minimum holding time, t_{hold}, after the clock edge. Present RAMBUS standards call for symmetric t_{hold}, and t_{setup} of 190ps each, with the total 380ps period centered on the clock edge. Thus, a data value is held valid for a minimum of 380ps, i.e., the combined value of t_{hold}, and t_{setup}, leaving some margin time from the total data valid time period of 650ps to allow for errors in clock edge placement relative to a data value.

Load circuit 52 supports skewing of the clock signal to move clock edges relative to a constant or unskewed data value. Thus, by moving the clock signal relative to the data signal, load circuit 52 supports testing of t_{hold} and t_{setup} values to ensure compliance with minimum specifications, such as a length of 190ps for setup and hold time relative to an associated clock edge. Further, load circuit 52 allows programmable testing of various RIMM to channel controller trace lengths by skewing of the clock signal to mimic delays introduced with greater trace lengths. An oscillator 202 provides a base time signal to direct RAMBUS clock generator (DRCG) 31. DRCG 31 uses the base clock signal to generate two RAMBUS clock timing signals that are 180 degrees out-of-phase with each other. The two out-of-phase clock signals are each at t_{clk} of 400 MHz, and allow more precise definition of clock edge placement in light of potential inaccuracies such as may result from clock transition rise times.

DRCG 31 provides the clock timing signal to DUT 26 and channel controller 34 to allow transfer of data to and from a RIMM associated with DUT 26. The timing clock signal supports the transfer of test write data from channel controller 34 to DUT 26 and read test data from DUT 26 to channel controller 34 at predetermined clock edges. Load circuit 52 allows the skewing or adjustment

of the timing clock signal relative to a constant or unskewed data write or read signal.

Load circuit 52 includes two programmable delay circuits, a write data programmable delay circuit 204 and a read data programmable delay circuit 206. Write data programmable delay circuit 204 adjusts the setup and hold timing of write test data transferred from channel controller 34 to be read by DUT 26. Read data programmable delay circuit 206 adjusts the setup and hold timing of read test data transferred from DUT 26 to be read by channel controller 34. Pin driver buffers 208 associated with each programmable delay circuit shifts voltage levels proceeding from each programmable delay circuit to desired levels. Pin driver buffers 208 support formation of varied clock edge shapes. A timing buffer 210 supports conversion from a differential clock to a single clock if needed.

In operation, the clock signals at point 212 of load circuit 52 are used by DUT 26 to time the driving of read data to controller 34, and by controller 34 to capture the read data. The clock signal at point 212 is delayed before being presented to controller 34 by a static duration determined by the insertion propagation delay of timing buffer 210, programmable delay circuit 204, and pin driver 208, and by a variable delay programmed into programmable delay circuit 204. The amount of variable delay programmed into 204 is determined during system calibration to result in controller 34 capturing the data driven by the DUT at the specified clock-to-output (t_Q) duration. When both minimum clock-to-output duration ($-t_Q$) and maximum clock-to-output duration ($+t_Q$) specifications need to be verified, testing is performed twice, with different programmable delays programmed into programmable delay circuit 204.

Clock signals at point 212 are buffered by timing buffer 210 and then routed through programmable delay

circuit 206 and pin driver 208 to drive the DUT via clock signals at point 214 of load circuit 52. The clock signal at point 214 is used by DUT 26 to capture transaction commands and write data driven by the controller 34. In operation, clock signals at point 214 are duplicates of clock signals at point 212 delayed by a static duration determined by the insertion propagation delay of timing buffer 210, programmable delay circuit 206, and the associated pin driver 208, and by a variable delay programmed into programmable delay circuit 206. The amount of variable delay programmed into programmable delay circuit 206 is determined during system calibration to result in the commands and data driven by controller 34 to lead (by t_{SETUP}) for setup time testing, or lag (by t_{HOLD}) for hold time verification, the edges of clock signals at point 214 by the specified amount. When both t_{SETUP} and t_{HOLD} specifications need to be verified, testing is performed twice, with different programmable delays programmed into programmable delay circuit 206.

Referring now to FIGURE 2, a block diagram depicts a stand-alone configuration of RIMM adapter 10 that is operationally independent of a separate hardware-enhanced test system. Test transaction engine 12 interfaces with a personal computer 24 for accepting user inputs and displaying test results, and also interfaces with ASIC 30. Test transaction engine 12 dispatches transactions specified in instruction SRAM 54 to DUT 26 through ASIC 30, and verifies data resulting from those transactions.

Test transaction engine 12 includes instruction SRAM 54, a sequencer 56 and function specific blocks including PMU 20, read compare engine 58, write generate engine 60, and address control generate engine 62. Instruction SRAM 54 accepts instructions loaded from personal computer 24 for use by transaction engine 12. Sequencer 56 communicates with personal computer 24 and instruction

SRAM 54 to supply addresses to instruction SRAM 54 in a user-defined order. Instruction SRAM 54 provides instruction data to write generate engine 60 and address control generate engine 62 to generate desired transaction address, commands and write data for transfer to ASIC 30. Instruction data from instruction SRAM 54 also provides instruction data to read compare engine 58 enabling read compare engine 58 to verify transaction read data received from ASIC 30. Instruction data from instruction SRAM 54 specifies the type of transaction that will be issued to DUT 26. In addition, instruction data stored in instruction SRAM 54 directs sequencer 56 to modify the next address issued to instruction SRAM 54, and specifies how the test address, test write data and test read compare data are modified after a transaction is issued.

Instruction data from instruction SRAM 54 includes address generation instructions for address control generate engine 62. The address generation instructions direct address control generate engine 62 to supply 35 bits of test address data in five fields to ASIC 30, with the fields corresponding to two column addresses, a row address, a bank address, and a device address. In addition, the instruction data directs address control generate engine 62 to issue a nominally 6 bit wide transaction command. Write generate engine 60 supplies either one or two 144 bit datums for each transaction command. In this way, the sequencer 56, address command generate engine 62 and write generate engine 60 provide a full speed data stream to facilitate full utilization of RAMBUS channel 28, with full control of transaction sequences issued to DUT 26 without constraint by microprocessor or memory controller implementations of test transaction engine 12.

Read compare engine 58 receives instruction data from instruction SRAM 54 enabling comparison of 144-bit

transaction read data received from ASIC 30 with expected values based on the nominally 6-bit wide transaction command provided by address command generate engine 62. Read compare engine 58 issues results for the comparison to sequencer 56 and personal computer 24, enabling a determination of the operational status of a RIMM in DUT 26. Read compare engine 58 includes a transaction command FIFO to account for access latencies of DUT 26 while performing reads. The FIFO of read compare engine 58 maintains a transaction command until the transaction to DUT 26 associated with the command is completed.

ASIC 30 includes address control FIFO 52 in communication with address control generate engine 62 and channel controller 34. Channel controller 34 maintains the status of active transactions with DUT 26 and the operational status of RDRAM devices loaded on a RIMM in DUT 26. Channel controller 34 extracts transaction address and control commands from address control FIFO 52, when RAMBUS channel 28 is available. A write FIFO 38 is in communication with write generate engine 60 and channel controller 34 so that, in the case of write transactions, up to 288 bits of write data can be transferred from write FIFO 38 by channel controller 34 when RAMBUS channel 28 is available. Read FIFO 36 is in communication with read compare engine 58 and channel controller 34 to allow channel controller 34 to load read transaction data returned from completed read transactions of DUT 26. Channel controller 34 communicates with RAC 32 and controls the transfer of data from and to RAC 32 through channel 28.

Read FIFO 36, write FIFO 38 and address command FIFO 52 form the interface between channel controller 34 of ASIC 30 and transaction engine 12. ASIC 30 provides a path by which reads and writes initiated through sequencer 56 can be accomplished. Status registers 64 internal to ASIC 30 allow test transaction engine 12 to

modify operational characteristics of channel controller 34 and RAC 32. ASIC 30, with Direct RAMBUS clock Generator (DRCG) 31 also implements RAMBUS channel input and output differential clocks and serial interface with channel clock circuit 66.

Referring now to FIGURE 3, a block diagram of address control generate engine 62 is depicted in a field programmable gate array (FPGA) embodiment. Address control generation engine 62 includes five logic blocks that accept predetermined transaction instructions from a user and provide test address and test control data to RIMM adapter 10. A bank block 70 provides 5-bit bank address data generated with a bank arithmetic logic unit (ALU) 72. Four bank registers 74 are selectable on a real-time basis for pipelined generation of DUT test bank addresses. A row block 76 provides 12-bit row addresses generated by a row ALU 78 and output by ROW register 82. Row block 76 includes a row comparator 80 and an end register 82 for determining when the final row address is generated. A column A block 84, including a column A ALU 86 and COLA register 90, and a column B block 92, including a column B ALU 94 and COLB register 96, generate 6-bit test column addresses. Column A comparators 88 and end registers support detection of two column address termination conditions. Hold registers 98 provide value storage capability for row block 76, column A block 84 and column B block 92. The fifth block of address control generation engine 62 is block 100, which provides five bits of device test with a device address with a device ALU 102 and four device address registers 104.

The logic blocks of address command generation engine 62 provide algorithmically-determined addresses to a RIMM on a per-access basis. The blocks accept instructions specified by a user and allow modification of the address patterns in accordance with a test

algorithm without respect to actual address values. Registers associated with the blocks store user-determined address patterns following operations by the ALUs pending transfer of the user-supplied addresses to the RIMM. The four bank address registers 74, device registers 104, column address bank 62 and column address bank 92 support storage of multiple instances of addresses to provide full speed multiple device transactions with the RIMM. For instance, the use of four registers for bank and device addresses allows intermingling of up to sixteen transactions to different addresses while accessing a RIMM. The use of multiple registers allows interleaved access of unique addresses to multiple devices on a RIMM, while also allowing multiple banks to be accessed in a single device. To accomplish interleaved access, a 2-bit field selects one of the four registers, and another 2-3 bit field selects the ALU operation to be performed on the selected register at the next clock edge. The register select field can be selected in advance of the operation selection by one selection cycle, allowing sufficient time to select the register and set up the value in that register to the ALU.

Referring now to FIGURE 4, a block diagram depicts a read compare engine 58 embodied as a FPGA. Read compare engine 58 includes circuits functionally equivalent to those found in write generate engine 60 in order to facilitate the comparison of data returned from DUT 26 to data written to DUT 26 during an earlier transaction that was generated by write data generation engine 60. Write generate engine 60 receives instructions by a sequencer or personal computer that modify hold registers 110 and offset register 112 for generating test write data with ALU 114. The test write data is provided to value registers 116 for transfer to a RIMM or, when instantiated inside of the read compare engine 58, for

use to compare against test read data received from a RIMM. Mask circuit 118, compare circuit 120 and error circuit 122 provide a comparison between test write data and test read data to detect differences that indicate an error with the RIMM that provided the test read data.

Referring now to FIGURE 5, a block diagram of address cross-bar switch 44 is depicted. Address cross-bar switch 44 eliminates unused bits from inputs A00 to A34, thus improving test efficiency by mapping address bits to channel controller 34 in contiguous fields. Address cross-bar switch has thirty-five inputs A00 through A34 and thirty-five outputs Ynn. Each input is provided to thirty-five address logic blocks 45 for each output Ynn. At most one logic block 45 associated with each output Ynn is selected, determining which input is gated to that output Ynn. Address cross-bar switch 44 can also reduce test time by simulating a vector-based test method and can sequence a given test data through a series of addresses by mapping address lines to different banks or devices on a RIMM under test. The sequencing of addresses enhances test efficiency with increased utilization of a channel of a RIMM under test and may also assist in the isolation of certain internal RIMM fault modes.

Referring now to FIGURE 6, a channel bypass circuit is conceptually depicted that supports additional testing of a RIMM under test. Address/command FIFO 40 interfaces directly with channel controller 34, or alternatively, interfaces directly with RAC 32 through a bypass circuit 53. Bypass circuit 53 allows a user to directly access RAC 32, enabling a user to send packets of test data to RAC 32 for performing additional tests not supported by channel controller 34. For instance, bypass circuit 53 allows a user to arrange certain bits sent to a RIMM and to perform tests of the low power mode of a RIMM. More thorough testing of a RIMM can be accomplished since

bypass circuit 53 provides direct control over every signal on the channel 28 at every clock edge of channel 28.

Referring now to Figure 7, a block diagram of one embodiment of a RIMM tester implementing the channel controller bypass is depicted. Input registers 64 of ASIC 30 receive information from test transaction engine 12, and the content of registers 64 may then be presented through channel controller 34 to RAC 32 or directly to RAC 32. If the test information is presented through channel controller 34, then channel controller 34 has the burden of issuing RAMBUS instructions, with a format and timing appropriate for the RIMM in DUT 26. If channel controller 34 is bypassed, then test transaction engine 12 provides data to drive RAC 32, such as transaction vectors and their related timing requirement, while channel controller 34 clocks return data from RAC 32. Bypassing channel controller 34 increases the complexity of the instructions of test transaction engine 12, and thus the software that generates the instructions. However, bypassing channel controller 34 allows greater control by test transaction engine 12 since channel controller 34 tends to select certain fixed methods for accomplishing memory operations and may not allow testing of certain unique sequences of commands.

Essentially, the components of the RIMM tester with a bypass circuit are functionally equivalent to like components discussed previously, however, in some instances, the test transaction engine communicates directly with RAC 32, bypassing channel controller 34. Host 24 downloads a high-level memory test algorithm which provides for variable assignments, arithmetic operations, looping, procedures, and flow control as well as access to specific command structures to a sequencer 56 through a portion of the SRAM 54. To enable direct communication with RAC 32, address control engine 62

provides 64 bit commands through registers 64 to RAC 32 in conjunction with 144 bit data. Thus, in summary, test transaction engine 12 provides information to RAC 32 on ASIC 30 in the same format as the data would have been provided if the data had come from channel controller 34.

To allow a comparison of the written data against subsequently read data, SRAM 54 provides very long instruction word (VLIW) instructions to sequencer 56. Sequencer 56 then provides the instructions to the address control engine 62, read/compare engine 58 and write engine 60, which use the instructions to generate the 64 bit commands and 144 bit data for writing through RAC 32. The address/control engine 62, read/compare engine 58 and write engine 60 generate command, data, timing and address sequences for ASIC 30 and for comparison of data read through RAC 32. Thus, the same instructions may be used to generate write data as are used to generate read compare data.

In bypass mode, the output of address/control engine 62 is generally a sequence of RAC packet commands with associated timing information. For instance, RAC 32 may support ROW packets having three bytes of information and COL packets having five bytes of information. The packet commands are generally transmitted as a group of eight bytes at a 100 MHz rate, although some packets may not have valid data. To provide additional scheduling flexibility, packets within each group of eight bytes, as well as data reads and writes, may be scheduled at 2.5 nS increments within the 10 nS clock period. Timing offset information provided via the VLIW command word provides 8 bits of offset information with 2 bits each corresponding to four offset times for a row packet, a column packet, write data, and read data.

In FIGURE 7, vector, OP code & address and write mask paths have a total of 64 bits that represent packet data, although an application of names to specific pins

is somewhat artificial since the signal on any given pin depends on the particular mode and format of the current packet. Generally, however, the write mask path outputs 16 bits worth of data for either a COLM or COLX packet when in the vector mode of bypassing channel controller 34, and outputs a write mask when in the standard mode of processing instructions through channel controller 34. The OP code and address path provides 35 bits of address information, four op code bits and one bit of packet length when data is passed through channel controller 34. In the vector mode of bypassing channel controller 34, the 40 bits of path associated with OP code and address are combined with the 8 bits of path associated with the vector path and the 16 bits of path associated with the write mask to provide a 64 bit path to pass eight bytes of packet information. Note that, although FIGURE 7 depicts one embodiment of a bypass circuit, in yet another embodiment, test transaction 12 can perform all of the functions of channel controller 34, thus eliminating the need for a channel controller on ASIC 30.

Referring now to FIGURE 8, a flow diagram depicts one possible test flow for a RIMM associated with RIMM adapter 10. At step 150, the connectivity of all RIMM input and output signals and voltages is performed before power is applied to the RIMM under test. At step 152, quiescent RIMM power consumption is verified. At step 154, access to all RDRAMS on the RIMM is verified, with initialization performed by the CMOS serial bus. At step 156, all RDRAMs on the RIMM are verified as able to detect unique patterns on the row, column and data DQ[AB] buses, including refresh and current control performed at predetermined intervals. Upon completion of step 156, the basic connectivity of the RDRAMs on the RIMM is verified.

At step 158, the voltage levels on the data DQ[AB] signals are verified during burst reads of each RDRAM on

the RIMM. At step 160, write and read verification is accomplished for all cells in each RDRAM on the RIMM. Write and read verification includes worst-case condition testing under different voltage, loading and timing conditions. Pattern sensitivity tests are also accomplished if necessary. Refresh and current control are accomplished at predetermined intervals. At step 162, each channel transaction required for the target application is performed and validated. At step 164, the RIMM SPD EEPROMs are programmed and verified.

Although the present invention has been described in detail, it should be understood that various changes, substitutions and alterations can be made thereto without departing from the spirit and scope of the invention as defined by the appended claims.

WHAT IS CLAIMED IS:

1. An application specific integrated circuit for communicating test data between a test transaction engine and a RIMM associated with a RAMBUS Channel; comprising:

a RAMBUS ASIC Channel cell for providing test data to a RAMBUS channel and accepting test data from the RAMBUS channel;

a channel controller interfaced with the RAMBUS ASIC Channel cell, the channel controller for controlling the writing and reading of test data by the RAMBUS ASIC Channel cell in cooperation with a timing signal; and

a load circuit interfaced with the channel controller, the load circuit operational to adjust the timing signal by programmable time period relative to a constant data signal.

2. The application specific integrated circuit of Claim 1 wherein the load circuit supports testing of setup time for a data signal within a predetermined accuracy.

3. The application specific integrated circuit of Claim 1 wherein the load circuit supports testing of hold time for a data signal within a predetermined accuracy.

4. The application specific integrated circuit of Claim 1 further comprising at least one first-in-first-out circuit interfaced with the channel controller, the first-in-first-out circuit for accepting test data from the test transaction engine and providing test data to the test transaction engine.

5. A system for testing a RIMM, the system comprising:

a test transaction engine for generating and reading test transaction data to test the operation of the RIMM;

a RIMM adapter interfaced with the test transaction engine, the RIMM adapter for communicating test transaction data between the test transaction engine and the RIMM in cooperation with a clock timing signal; and

a programmable load circuit associated with the RIMM adapter, the programmable load circuit operational to adjust the clock timing signal to test hold time or setup time specifications by a programmable time period.

6. The system according to Claim 5 wherein the RIMM adapter comprises an ASIC having a RAMBUS ASIC Channel cell and a channel controller.

7. The system according to Claim 5 wherein the test transaction engine comprises a hardware-enhanced memory test system.

8. The system according to Claim 5 wherein the test transaction engine comprises a write data path for providing test write data to the RIMM adapter, and a read data path for accepting test read data from the RIMM adapter, the programmable delay circuit operational adjust the clock timing signal for either the read data path or the write data path.

9. The system according to Claim 5 further comprising a read compare engine for accepting test read data from the RIMM adapter and comparing the test read data against test write data to determine RIMM results.

10. A method for testing a RIMM comprising the steps of:

generating test transaction information;

providing the test transaction information to the RIMM in cooperation with a clock timing signal for storage of the test transaction data on the RIMM;

reading the stored test transaction information from the RIMM in cooperation with a clock timing signal;

adjusting the clocking timing signal by a programmable time period; and

comparing the test transaction information read from the RIMM against predetermined results to determine the operational status of the RIMM.

11. The method according to Claim 10 wherein the test data is written and read to the RIMM through a RIMM adapter comprising an application specific integrated circuit having a RAMBUS ASIC channel cell and a channel controller.

12. The method according to Claim 10 wherein the test transaction information comprises test write data.

13. The method according to Claim 11 wherein the providing the test transaction data to the RIMM step further comprises the steps of:

providing the test write data to the channel controller; and

using the channel controller to direct the RAMBUS ASIC channel cell to send the test write data to the RIMM.

14. The method according to Claim 11 wherein the comparing step further comprises the step of generating read compare test data with the instructions and a read compare engine for comparison with the data read from the RIMM.

15. The method Claim 10 further comprising the step of adjusting the clock timing signal by a predetermined setup time period.

16. The method of Claim 10 further comprising the step of adjusting the clock timing signal by a predetermined hold time period.

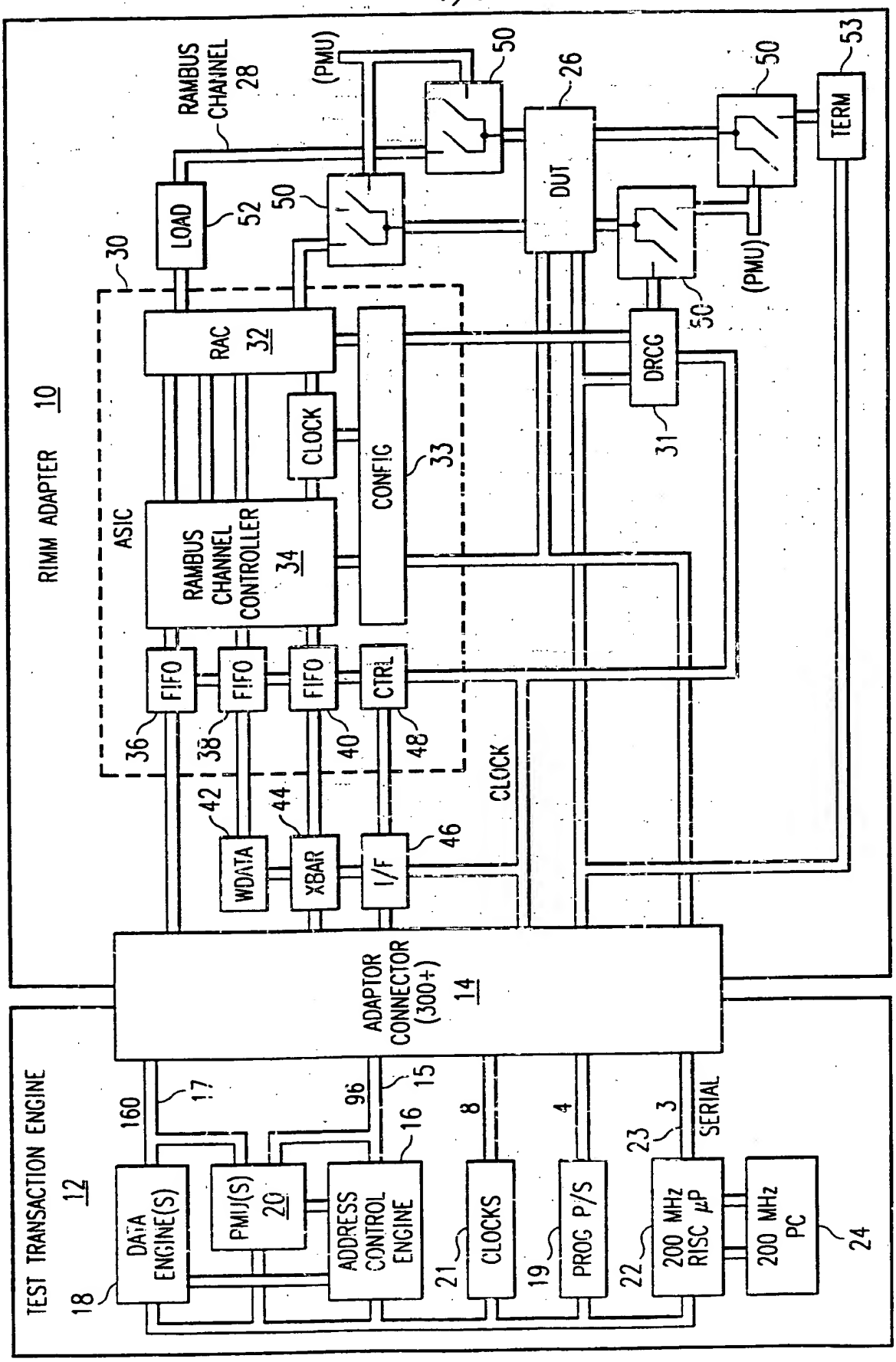

TEST TRANSACTION ENGINE
12
DATA ENGINE(S)
18
PMU(S)
20
ADDRESS CONTROL ENGINE
16
CLOCKS
21
PROG P/S
19
200 MHz RISC μP
22
200 MHz PC
24
160
17
96
15
8
4
23
3
SERIAL
ADAPTOR CONNECTOR (300+)
14
RIMM ADAPTER
10
ASIC
30
RAMBUS CHANNEL CONTROLLER
34
RAC
32
CLOCK
CONFIG
33
FIFO
36
FIFO
38
FIFO
40
CTRL
48
WDATA
42
XBAR
44
I/F
46
CLOCK
RAMBUS CHANNEL
28
LOAD
52
(PMU)
50
DUT
26
DRCG
31
TERM
53

FIG. 1

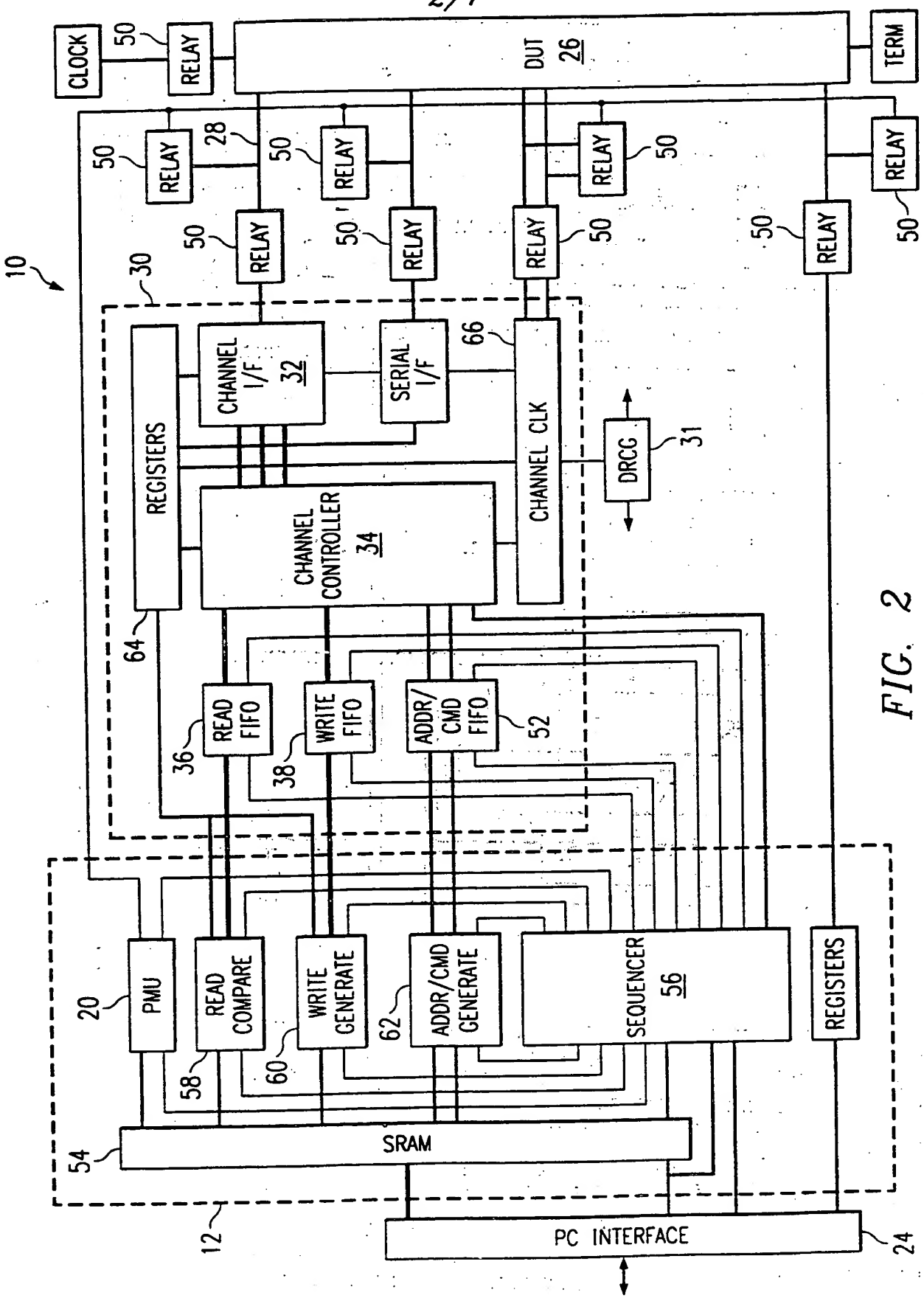


FIG. 2

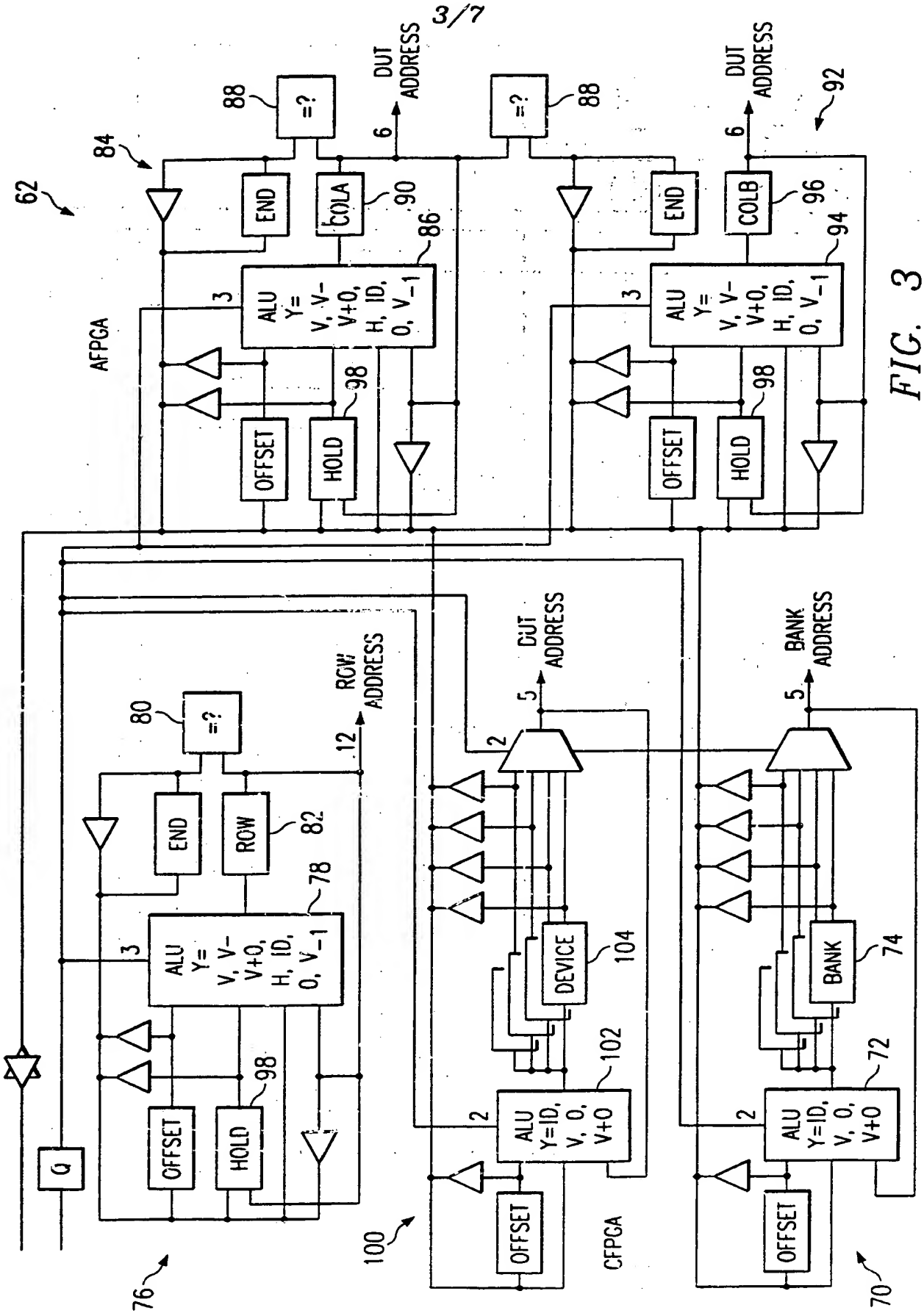


FIG. 3

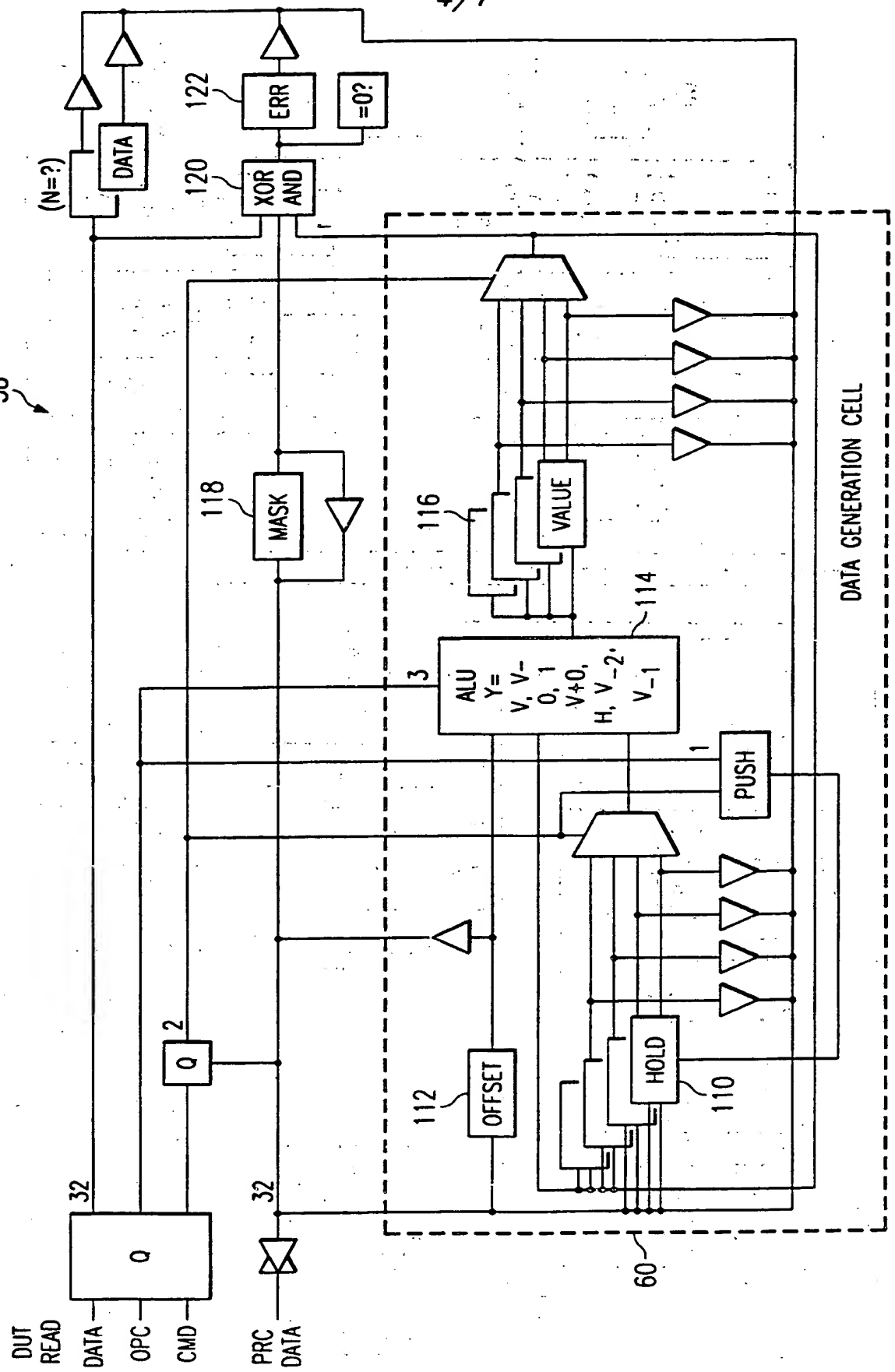


FIG. 4

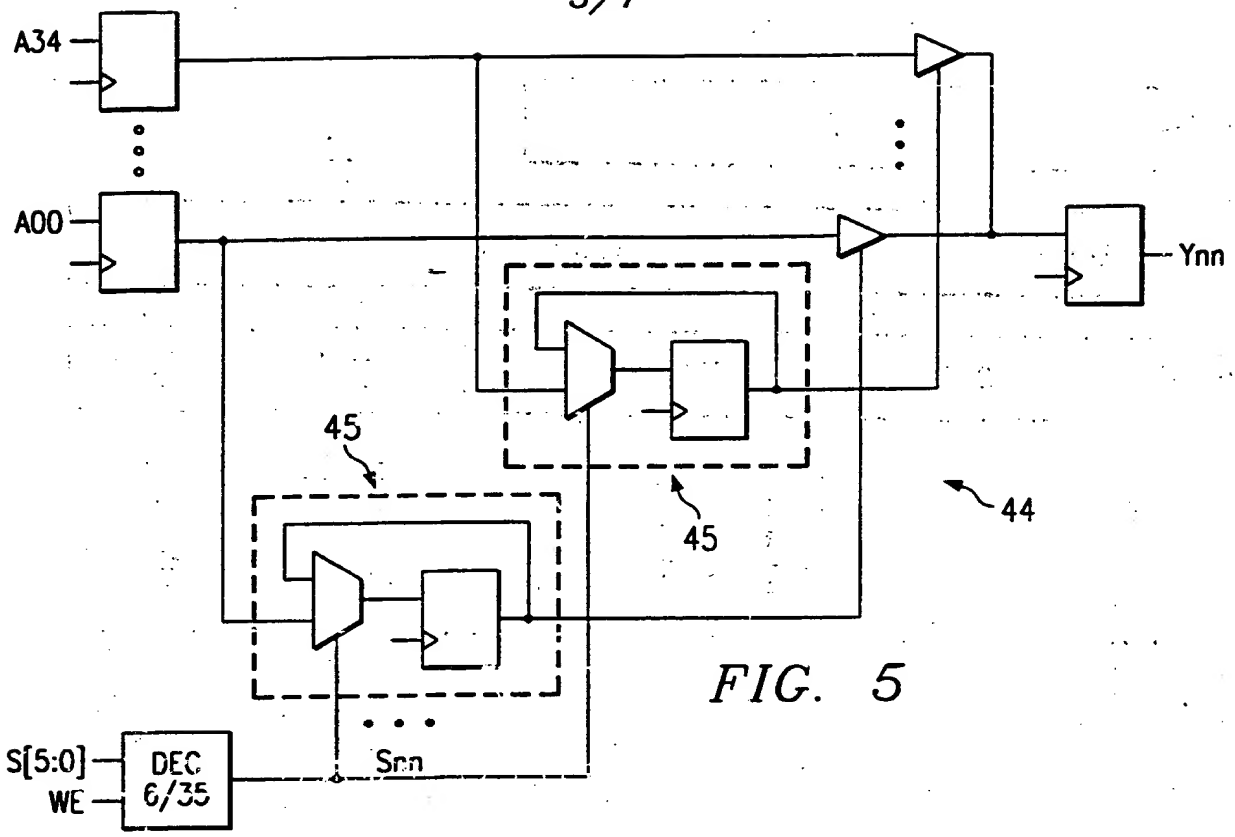


FIG. 5

FIG. 6

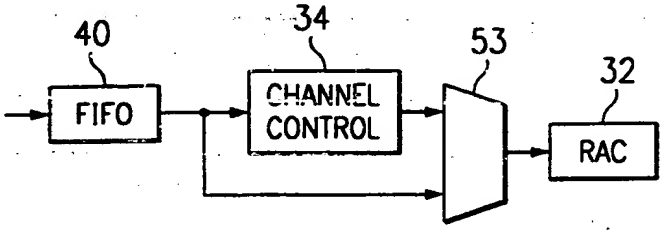


FIG. 8

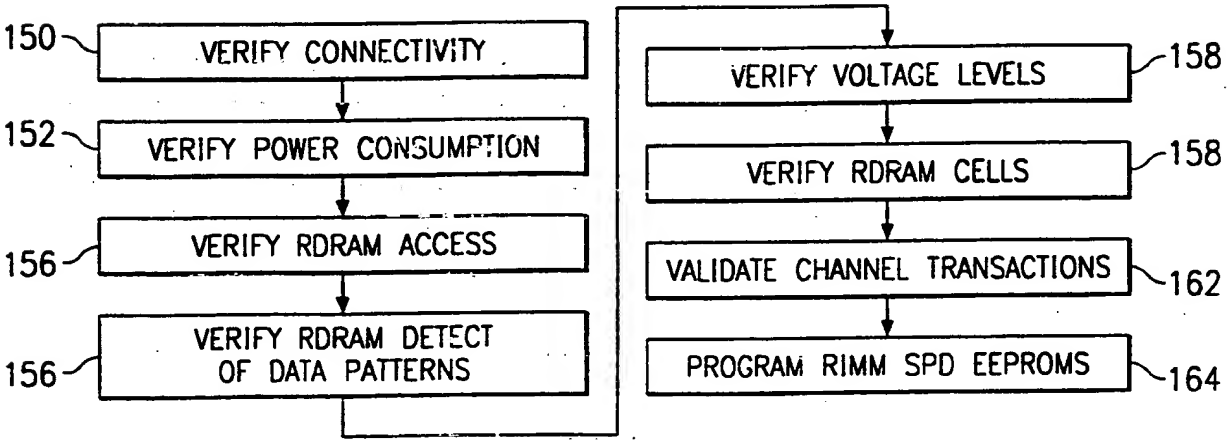
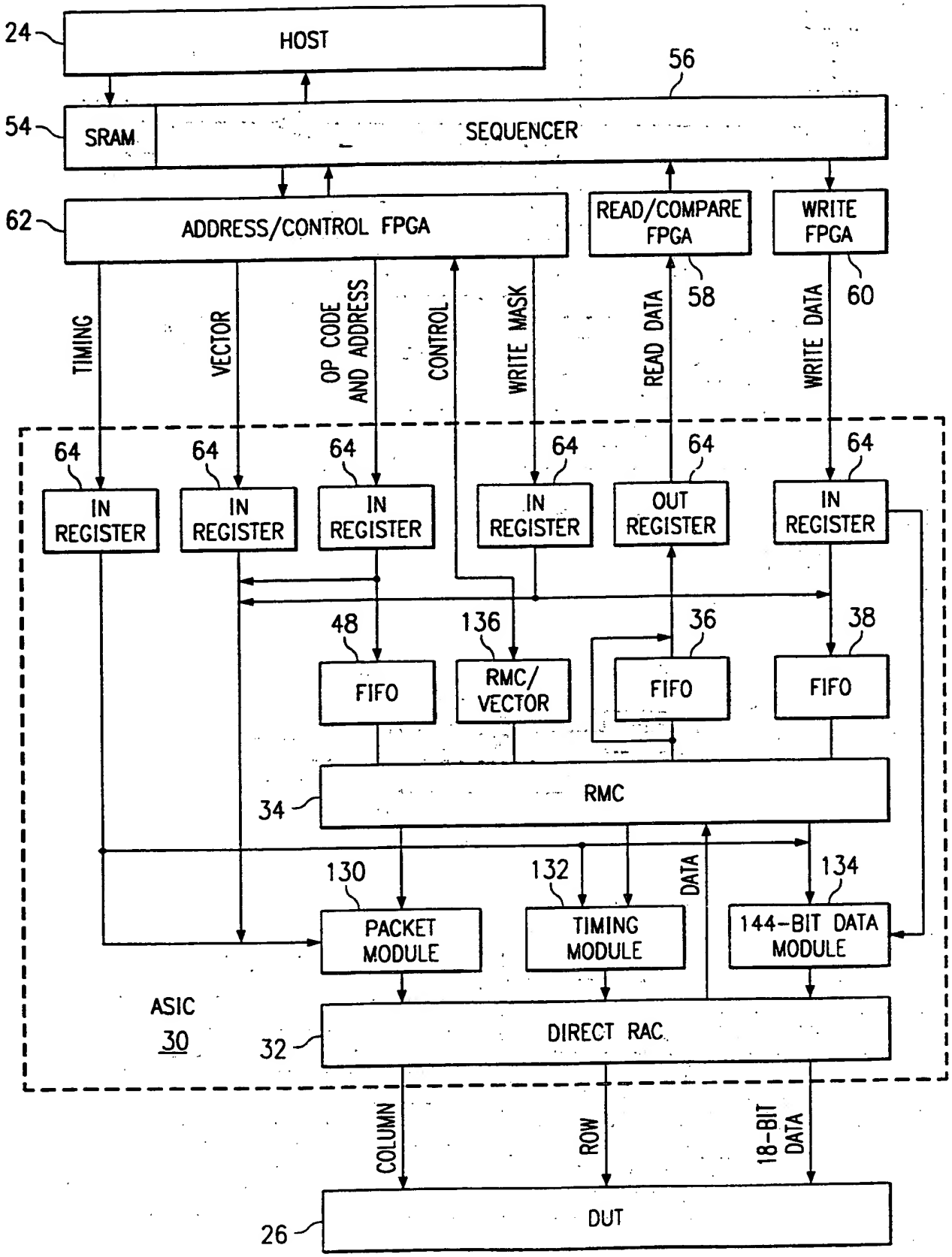


FIG. 7



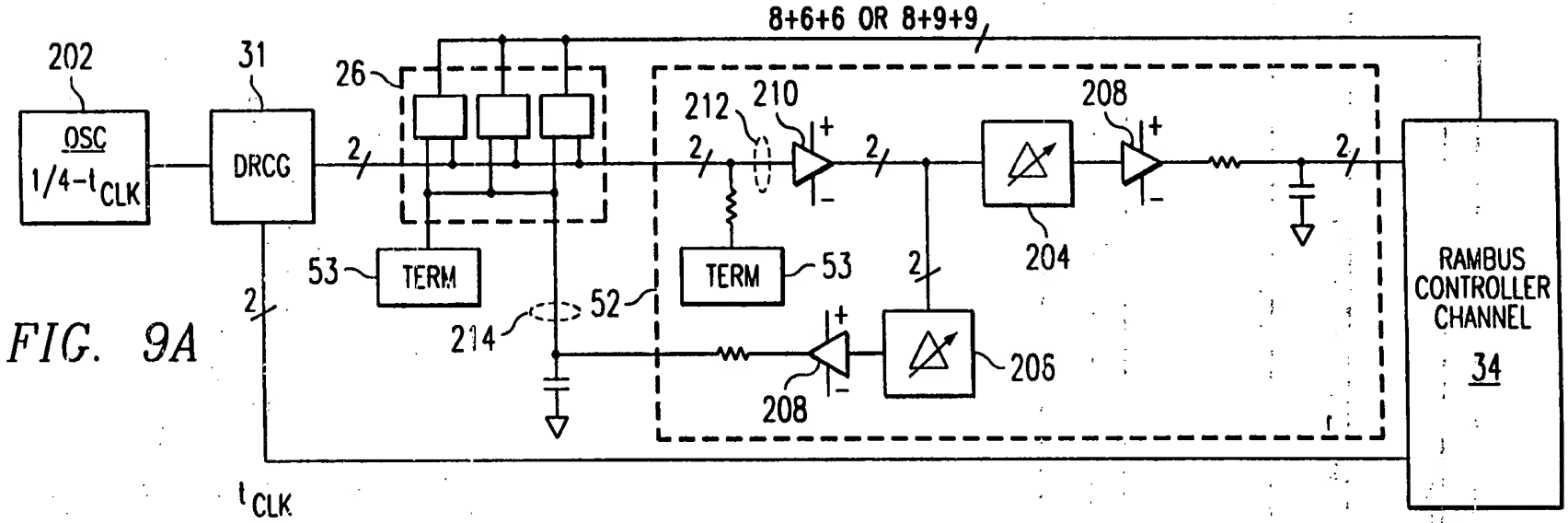


FIG. 9A

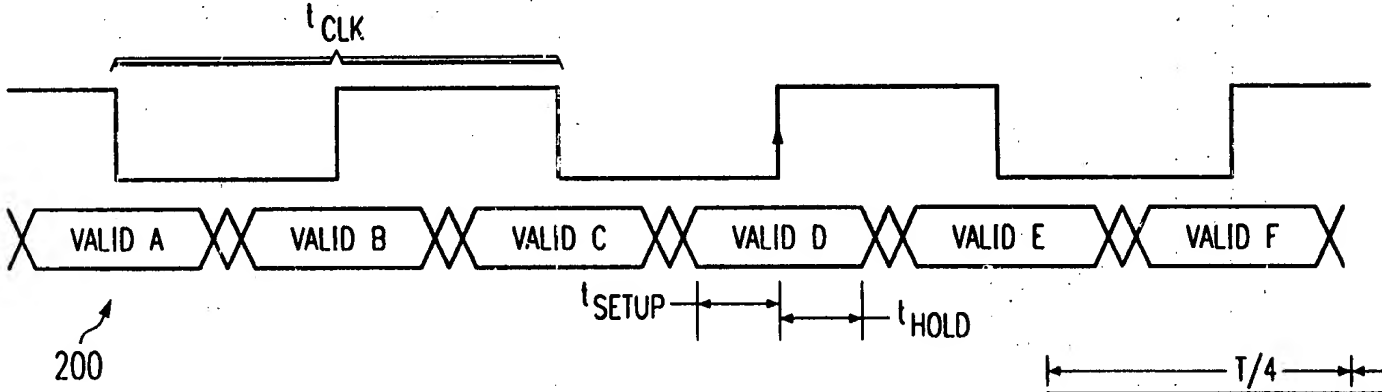


FIG. 9B

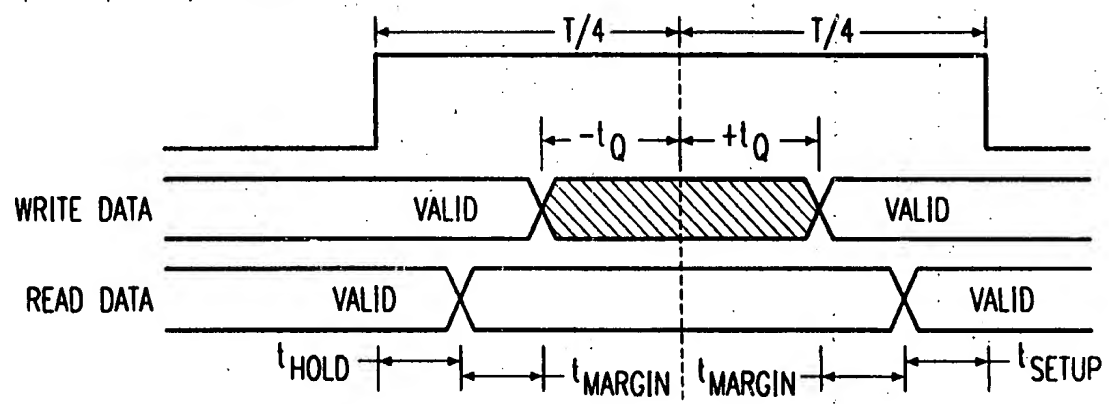


FIG. 9C

INTERNATIONAL SEARCH REPORT

International Application No
P../US 99/19752

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 G11C29/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 G11C G01R

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
P,A	HO C C: "Defining tomorrow's memory module tester" EE EVALUATION ENGINEERING, NELSON PUBLISHING, vol. 38, no. 3, March 1999 (1999-03), pages 14-18, XP002122524 USA figure 3 --- -/--	1-16

[X] Further documents are listed in the continuation of box C.

[ ] Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
12 November 1999	26/11/1999

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl. Fax: (+31-70) 340-3016	Huyghe, E

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Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

International Application No
PC./US 99/19752

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	GOLDBERG J M: "TIMING: THE KEY TO RAMBUS TESTING" TEST AND MEASUREMENT WORLD. (INC. ELECTRONICS TEST),US,CAHNERS PUBLISHING, DENVER; vol. 17, no. 11; 1 October 1997 (1997-10-01), page 53-54,56,58-59 XP000725991 ISSN: 0744-1657 the whole document	1-16
A	GASBARRO J A ET AL: "TECHNIQUES FOR CHARACTERIZING DRAMS WITH A 500 MHZ INTERFACE" PROCEEDINGS OF THE INTERNATIONAL TEST CONFERENCE,US,NEW YORK, IEEE, 2 October 1994 (1994-10-02), page 516-525 XP000520014 ISBN: 0-7803-2103-0	1-16

1

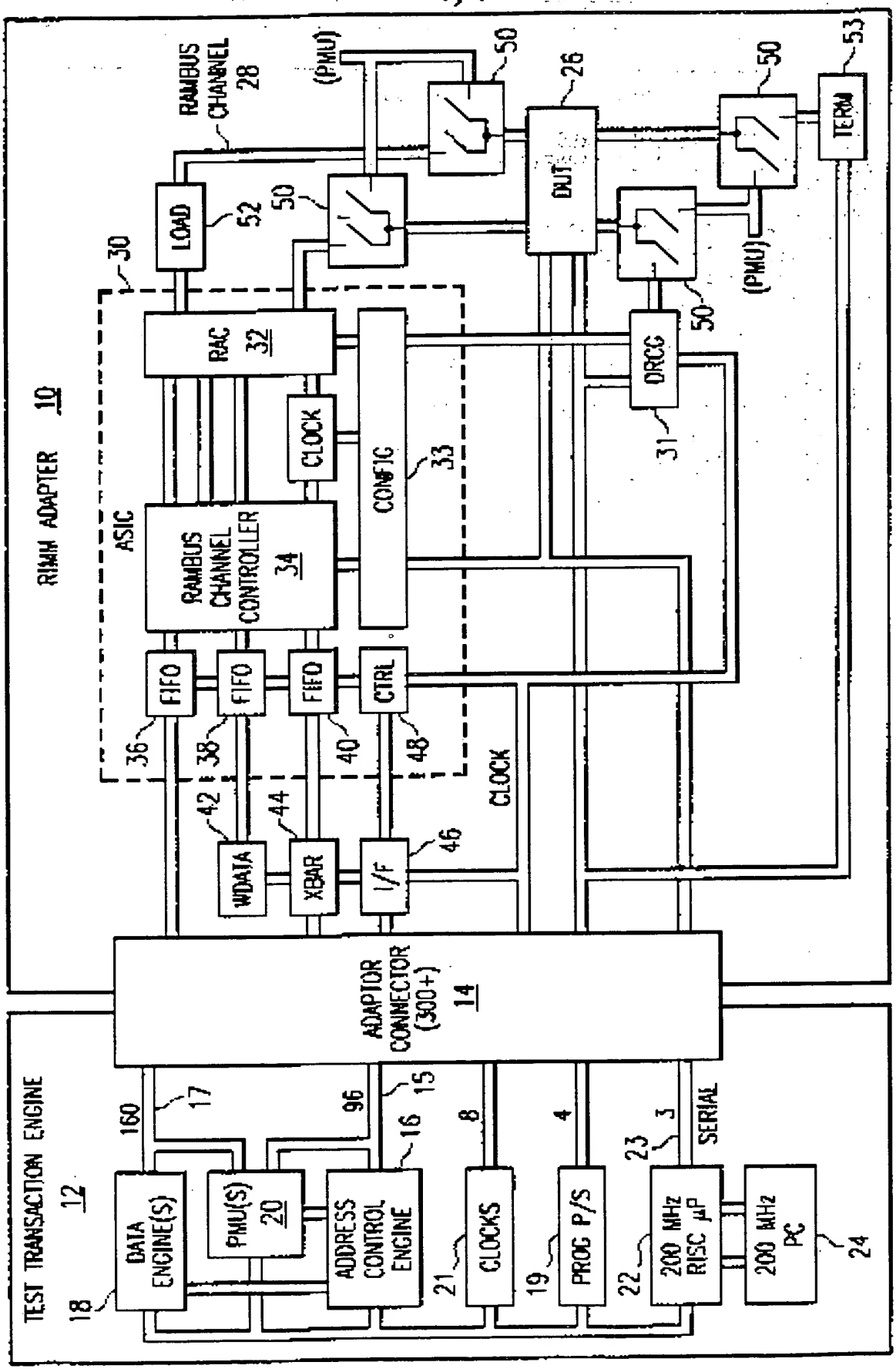
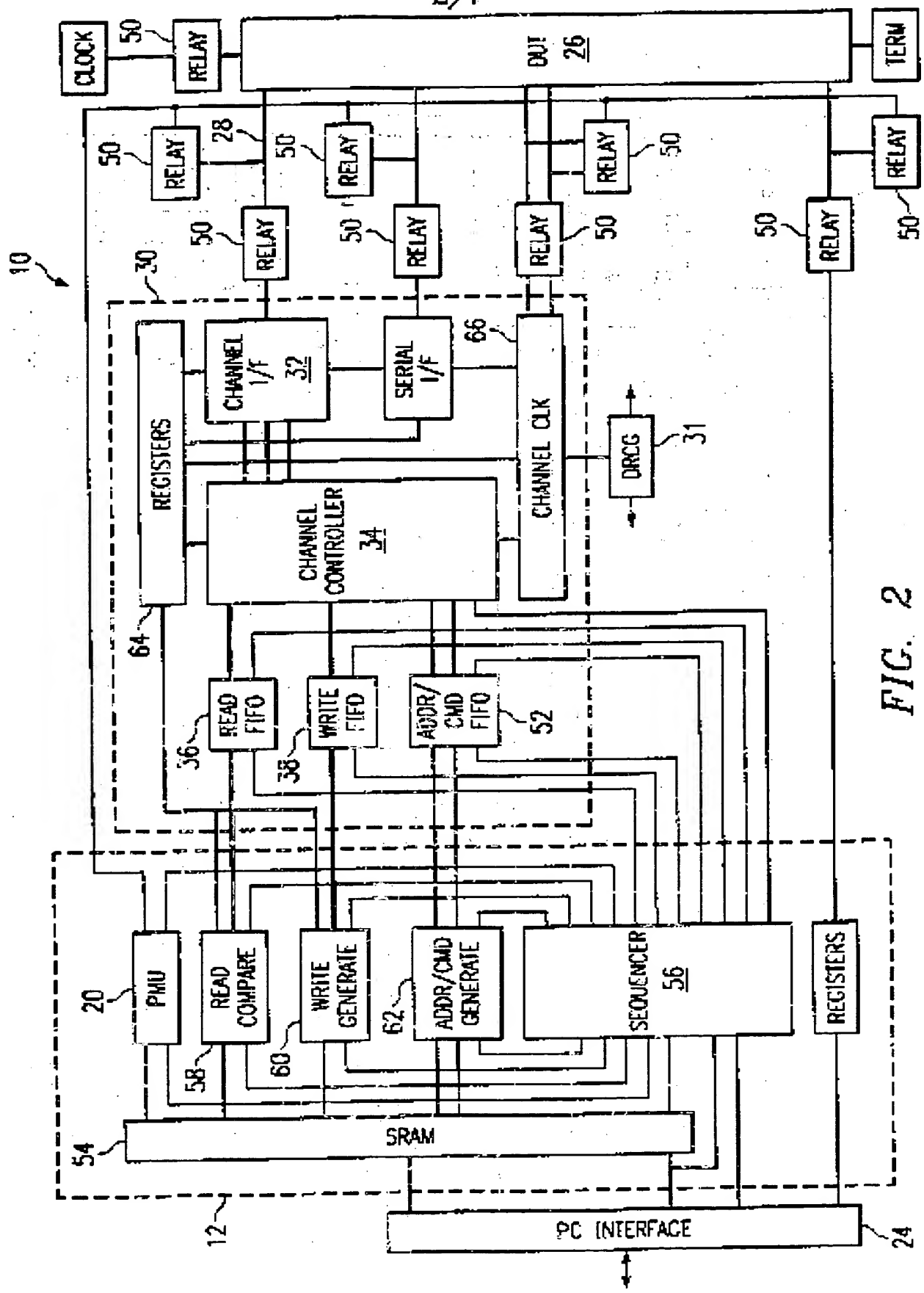


FIG. 1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RELAY
50
OUT
26
TERM
28
10
30
REGISTERS
CHANNEL I/F
32
SERIAL I/F
66
CHANNEL CLK
DRCG
31
CHANNEL CONTROLLER
34
64
READ FIFO
36
WRITE FIFO
38
ADDR/CMD FIFO
52
20
PMU
READ COMPARE
58
WRITE GENERATE
60
62
ADDR/CMD GENERATE
SEQUENCER
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REGISTERS
SRAM
54
12
PC INTERFACE
24

FIG. 2

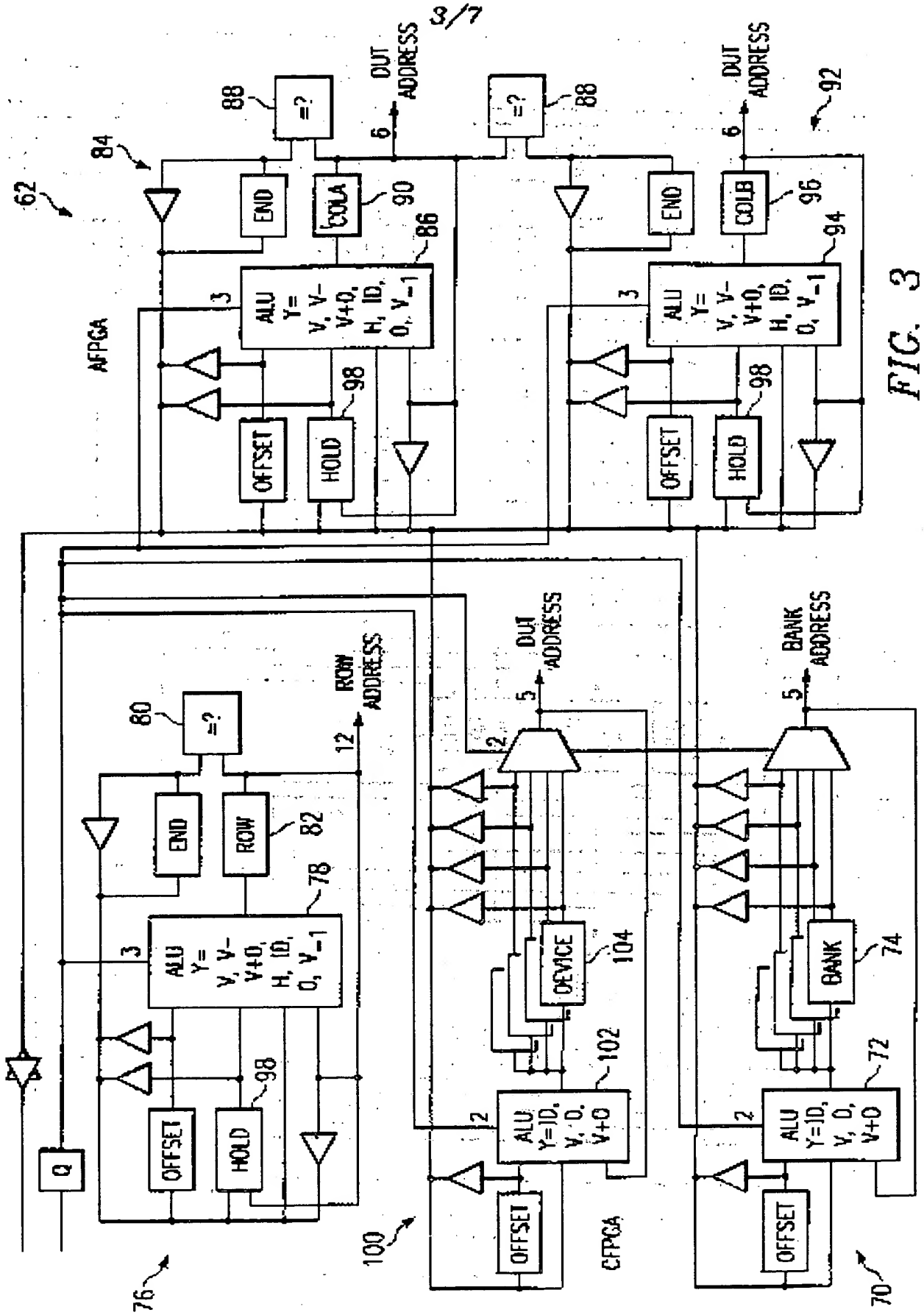


FIG. 3

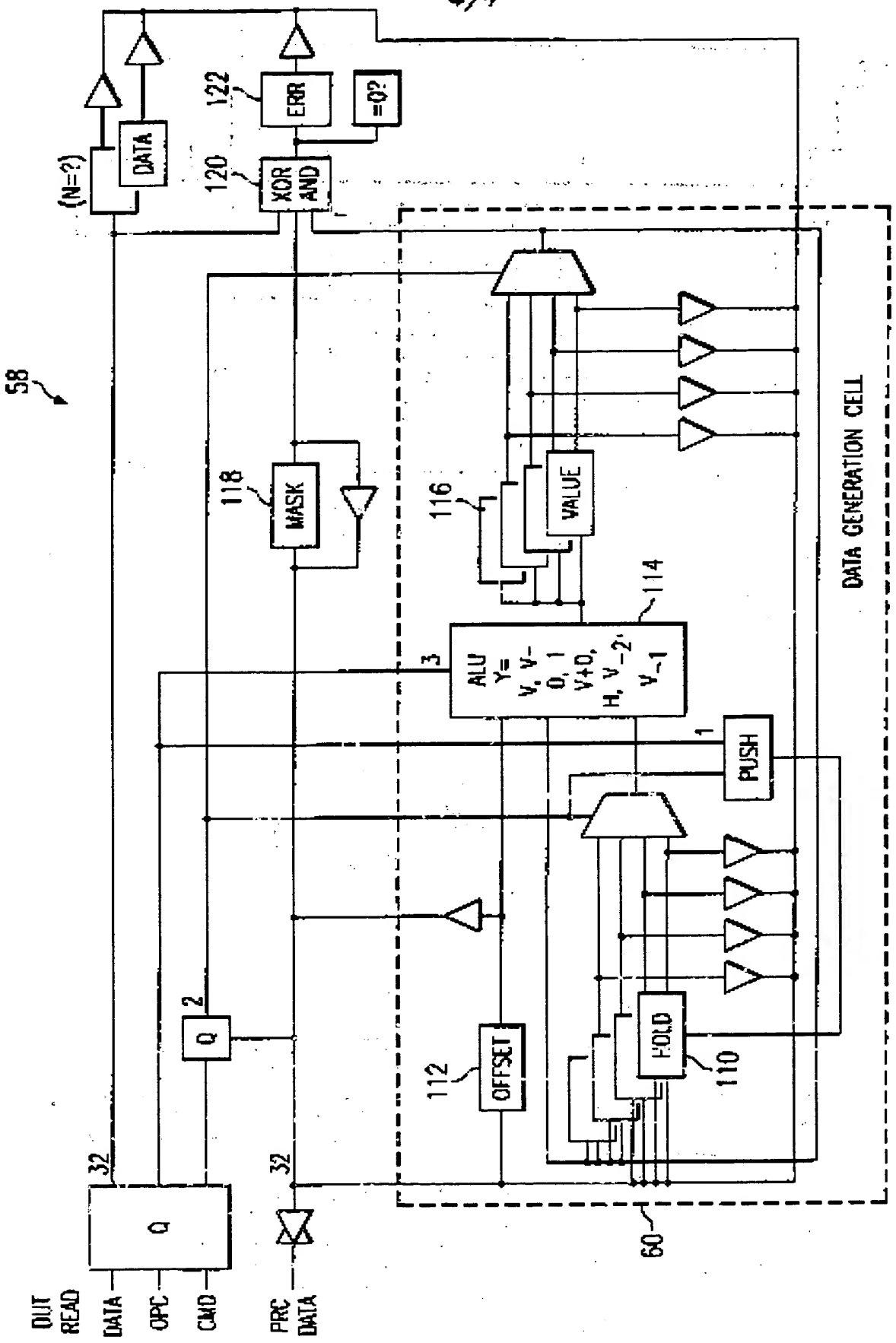


FIG. 4

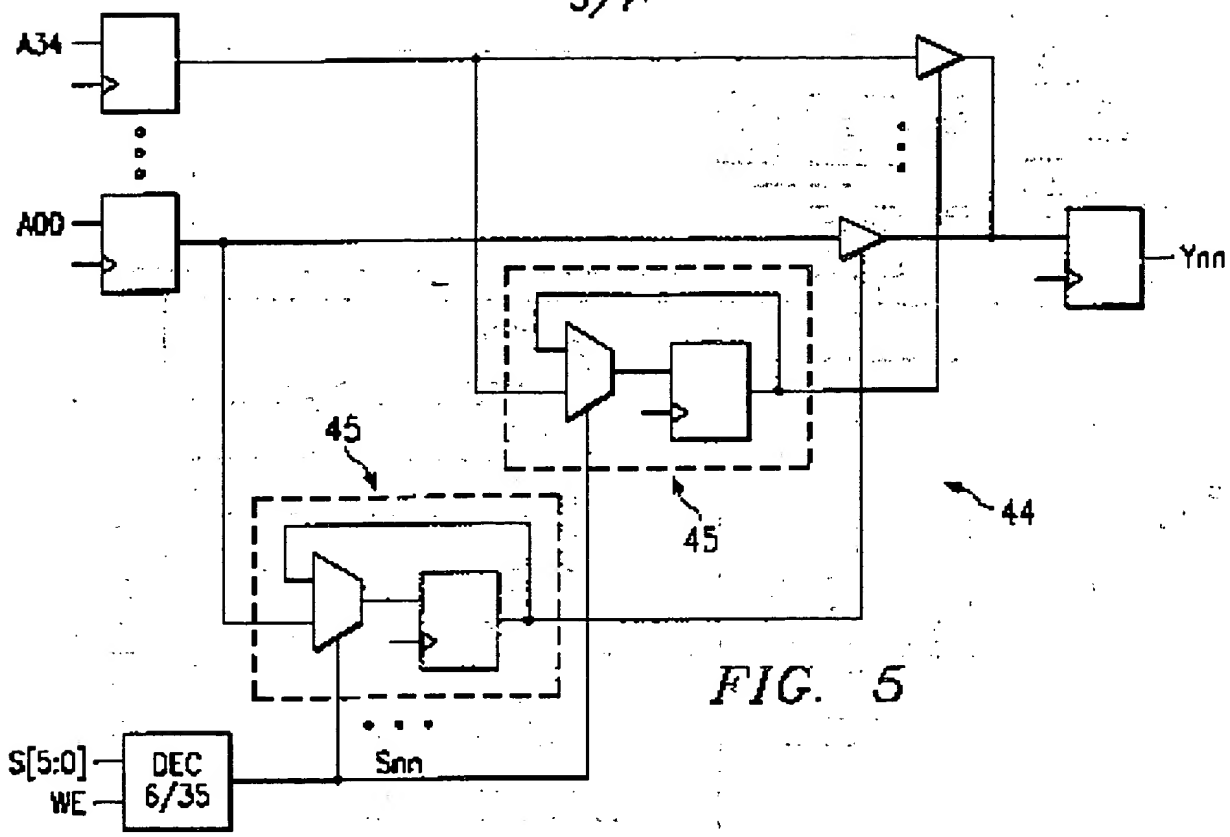


FIG. 5

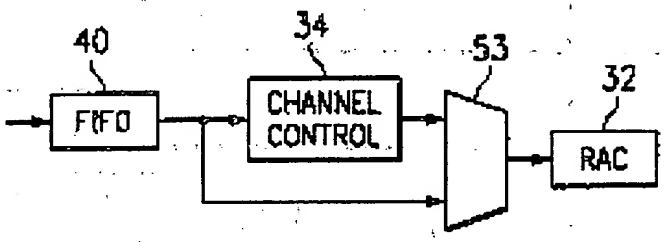


FIG. 6

FIG. 8

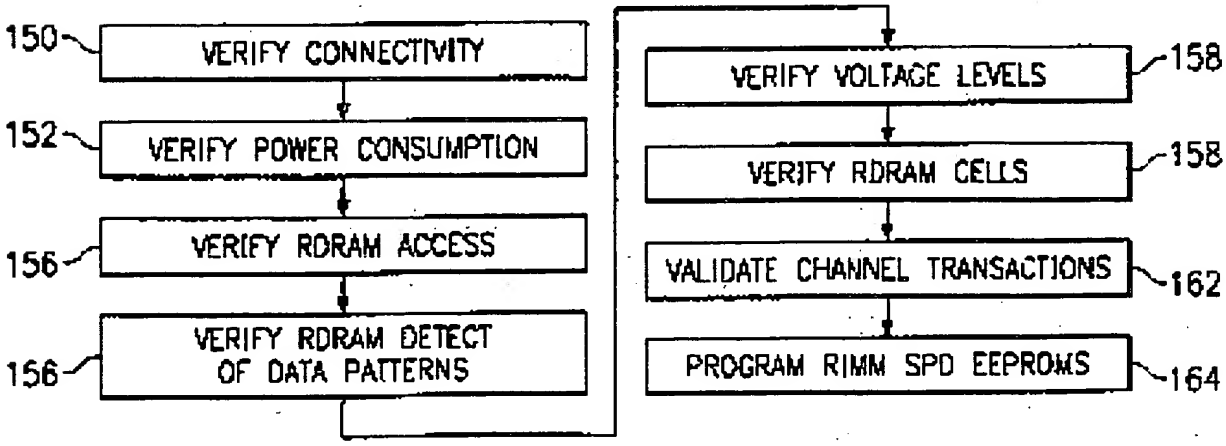
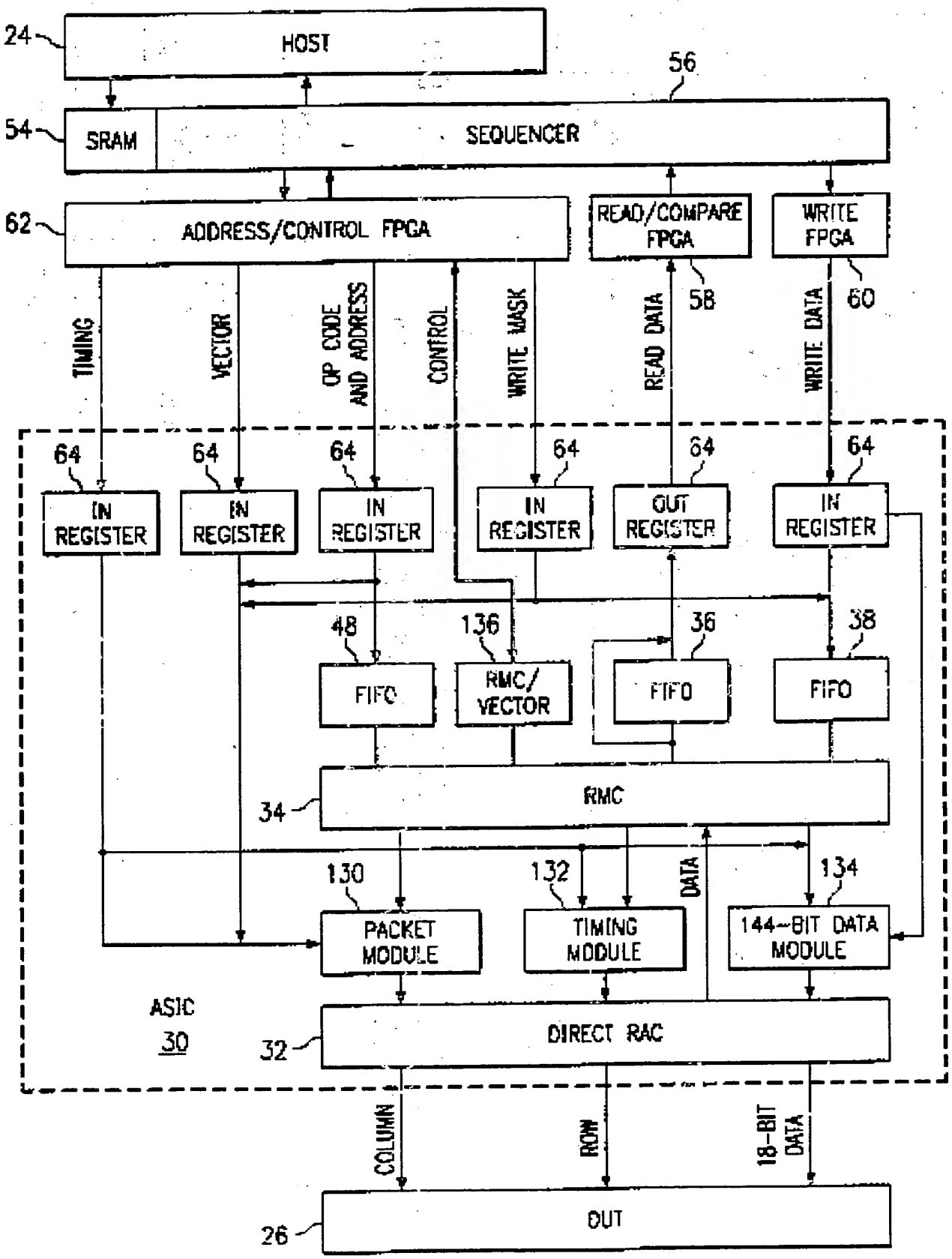


FIG. 7



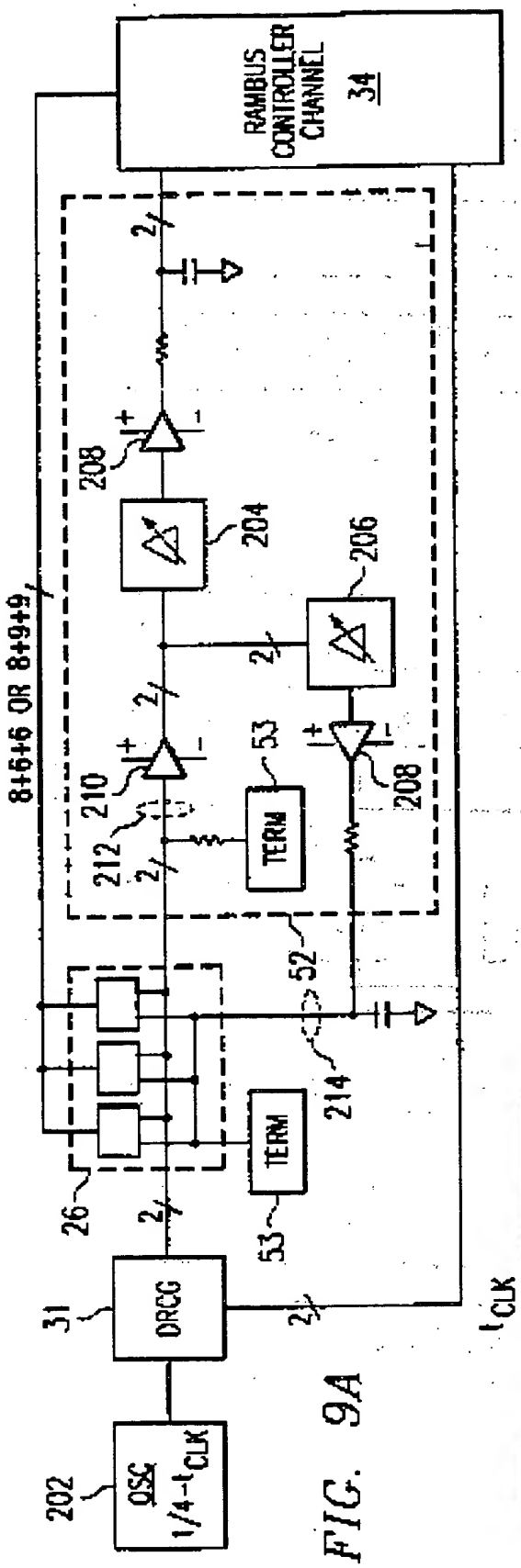


FIG. 9A

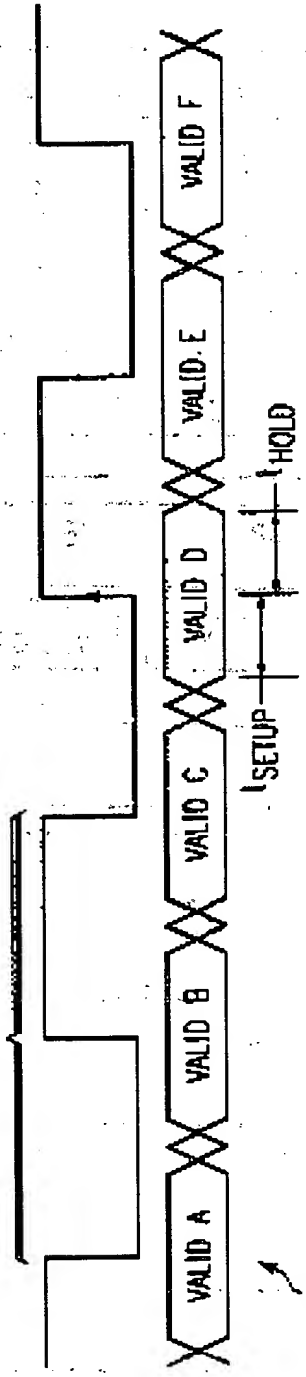


FIG. 9B

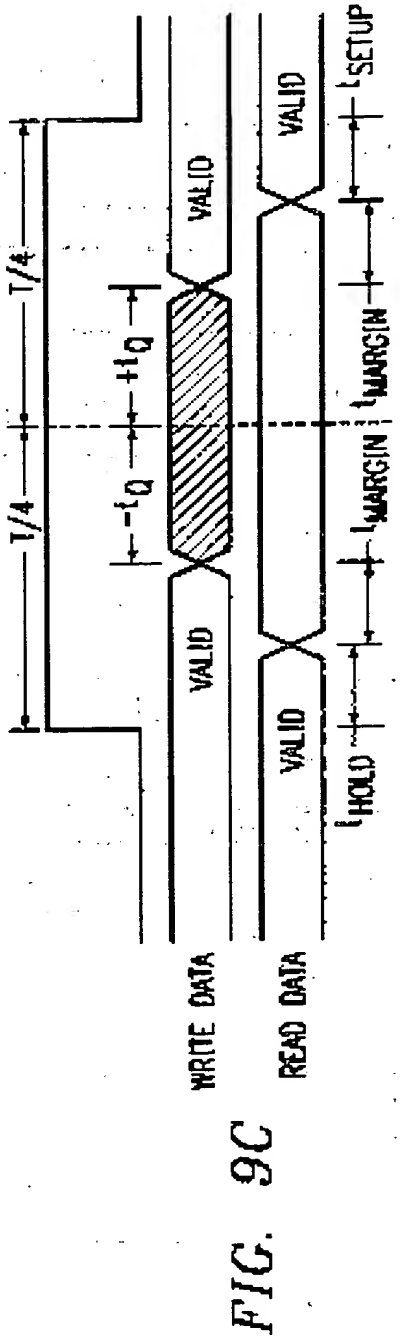


FIG. 9C